PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of	)	
	)	**For: COMPACT, LOW-POWER LOW-JITTER DIGITAL PHASE-LOCKED LOOP**
Amr Fahim	)	
	)	
	)	
Serial No. Unknown	)	
	)	
Filed: Herewith on August 19, 2003	)	

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(b)

Assistant Commissioner of Patents
Alexandria, VA 22313

Dear Sir:

Applicants submit herewith references of which they are aware in accordance with 37 CFR § 1.56.

In accordance with 37 CFR § 1.98 submitted herewith for consideration by the Examiner are the patents, publications and other information shown on the attached PTO-1449.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on:

August 19, 2003
(Date of Deposit)

Victoria J. Pacey
(Name of the Person Making Deposit)

(Signature)

The citation of these references is not intended to constitute an admission that any reference referred to herein is prior art to the invention of this application unless specifically designated as such.

The filing of this document shall not be construed to mean that any search has been made or, that if made, such search was complete or exhaustive, or that no other material information as defined in 37 CFR § 1.56 exists.

A list of the references cited herein is set forth on Form PTO-1449, which is enclosed herewith along with a copy of each cited reference. Applicants respectfully request that the Examiner return to Applicants the enclosed copy of the Form PTO-1449 indicating consideration of the references.

These references are being submitted prior to the issuance of the first Office Action. Therefore, it is believed that no fee is due for this submission.

Respectfully submitted,

Dated: August 19, 2003

By: _____
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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE (REV. 7-80) PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use several sheets if necessary)*	030284	Unknown
	APPLICANT: Amr Fahim	
DATE MAILED: August 19, 2003	FILING DATE: August 19, 2003	GROUP: Unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPRO-PRIATE
	A1						
	A2						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS
	B1						
	B2						

OTHER PRIOR ART (*Including Author, Title, Date, Pertinent Page, Etc.*)

	C1		Ahn, et al., "A Low-Jitter 1.9-V CMOS PLL for UltraSPARC Microprocessor Applications", IEEE Journal of Solid-State Circuits, Vol. 35, No. 3 March 2000 pps. 450 - 454
	C2		John Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11 November 1996, pps. 1723-1732
	C3		Wu, et al., "A Low Glitch 10-bit 75 MHz CMOS Video D/A Converter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 1, January 1995, pps. 68 – 72.
	C4		Chung, et al., "An All-Digital Phase-Locked Loop for High-Speed Clock Generation", IEEE Journal of Solid-State Circuits, Vol. 38, No. 2, February 2003, pps. 347 - 351
	C5		Hwang, et al., "A Digitally Controlled Phase-Locked Loop with a Digital Phase-Frequency Detector for Fast Acquisition," IEEE Journal of Solid-State Circuits, Vol. 36, No. 10, October 2001, pps. 1574 - 1581

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.